

SciEngines TiCore-FPGA-KIT



SciEngines GmbH · Schauenburgerstraße 116 · 24118 Kiel · Germany

Xilinx® Virtex®-5 FX Baseboard

Key Features

- Xilinx XC5VFX70T
- Xilinx XCF32P Platform Flash
- 10/100/1000 Ethernet PHY
- 16 MB Flash
- 64 MB DDR2 SDRAM
- Cypress USB 2.0 controller
- RS-232 serial port
- 2 x 16 character LCD
- EXP expansion slot (J4, J6)
- BPI configuration support
- 100 MHz oscillator (+ LVTTTL oscillator socket)
- System ACE interface
- User LEDs, DIP switch, and push-buttons

TriBoard TC1797 Baseboard

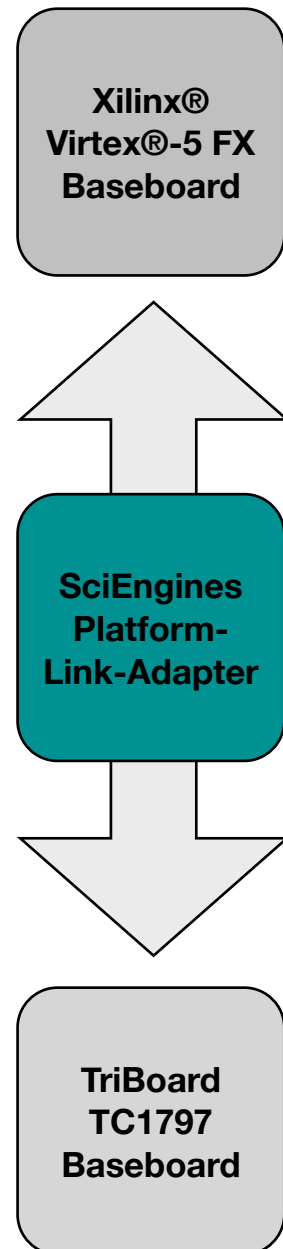
Key Features

- Infineon's TC1797 Controller
- Burst Flash up to 16MBytes
- asynchronous SRAM up to 1MByte
- FlexRay Transceivers (optional if not with TC1797)
- High Speed CAN Transceivers
- USB to UART bridge
- Crystal 20MHz (default), Oscillator or External Clock
- USB miniWiggler for easy debugging
- 8 Low Power Status LEDs
- 8-DIP switches for configuration

SciEngines Platform-Link-Adapter

Key Features

- Schematics
- Examples



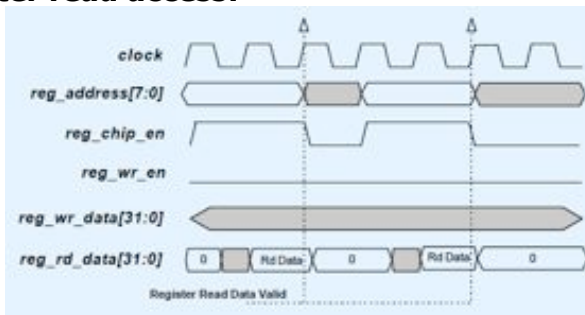
Principle I/O Description FPGA Register Interface

Register Bus Interface	
reg_address	8-bit address output A[0..7]
reg_chip_en	Block select input for the register bank.
reg_wr_en	Write Enable Input for block registers.
reg_wr_data	32-bit Write data input. (16-bit datainterface to tricore)
reg_rd_data	32-bit Write data output. (16-bit datainterface to tricore)
reg_irq	Interrupt / error

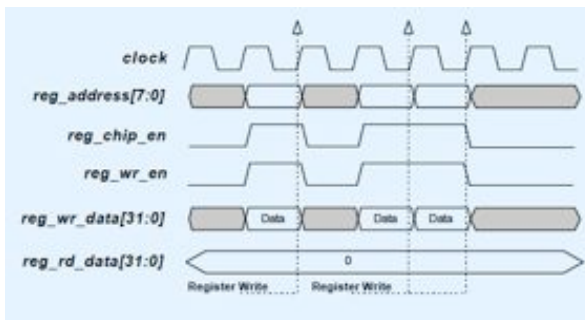
FPGA Register Interface

A simple 32-bit register-programming interface is provided. The register core is intended to be interfaced to whatever host interface is appropriate for the application (e.g. I₂C, 8-bit, big-endian, little-endian, etc).

Register read access:



Register write access:



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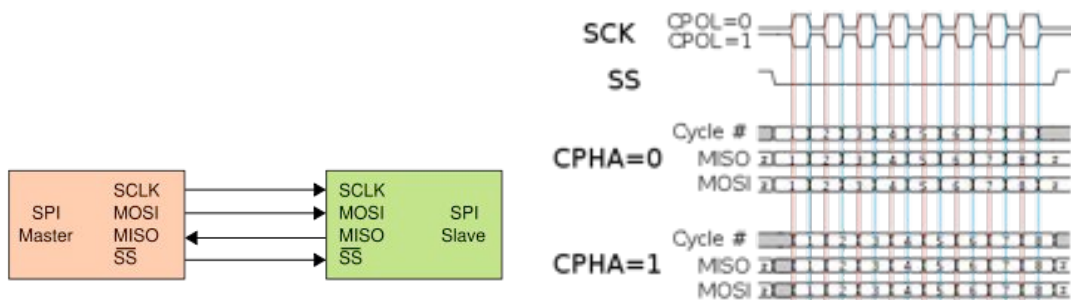
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Principle I/O Description SciEngines Platform-Link-Adapter

Register Bus Interface VHDL		FPGA-I/O PIN	TriCore TC1797 PIN
reg_address	8-bit address output A[0..7]	J4(44,46,48,50,52,54,56,58)	A[0..7]
reg_chip_en	Block select input for the register bank.	J4(60)	/CS0
reg_wr_en	Write Enable Input for block registers.	J4(6), J4(4)	/RD, /WR
reg_wr_data	32-bit Write data input.	J4(12,14,16,18,20,22,24,26,28,30,32,34,36,38,40,42)	D[0..16]
reg_rd_data	32-bit Write data output.	see above	see above
reg_irq	Interrupt / error	J4(8)	/WAIT
reg_clk	Register bus interface clock	J4(2)	CLK
spi_clk	SPI clock	J6(58)	SCLK
spi_mosi	SPI serial data output.	J6(60)	MOSI
spi_miso	SPI serial data input.	J6(62)	MISO
spi_ss	SPI select	J6(64)	/SS
spi_en	Enable SPI core.	internal	

SPI Interface

A hardware based SPI-Interface is provided interfacing the TriCore Baseboard and the Xilinx Virtex Baseboard.

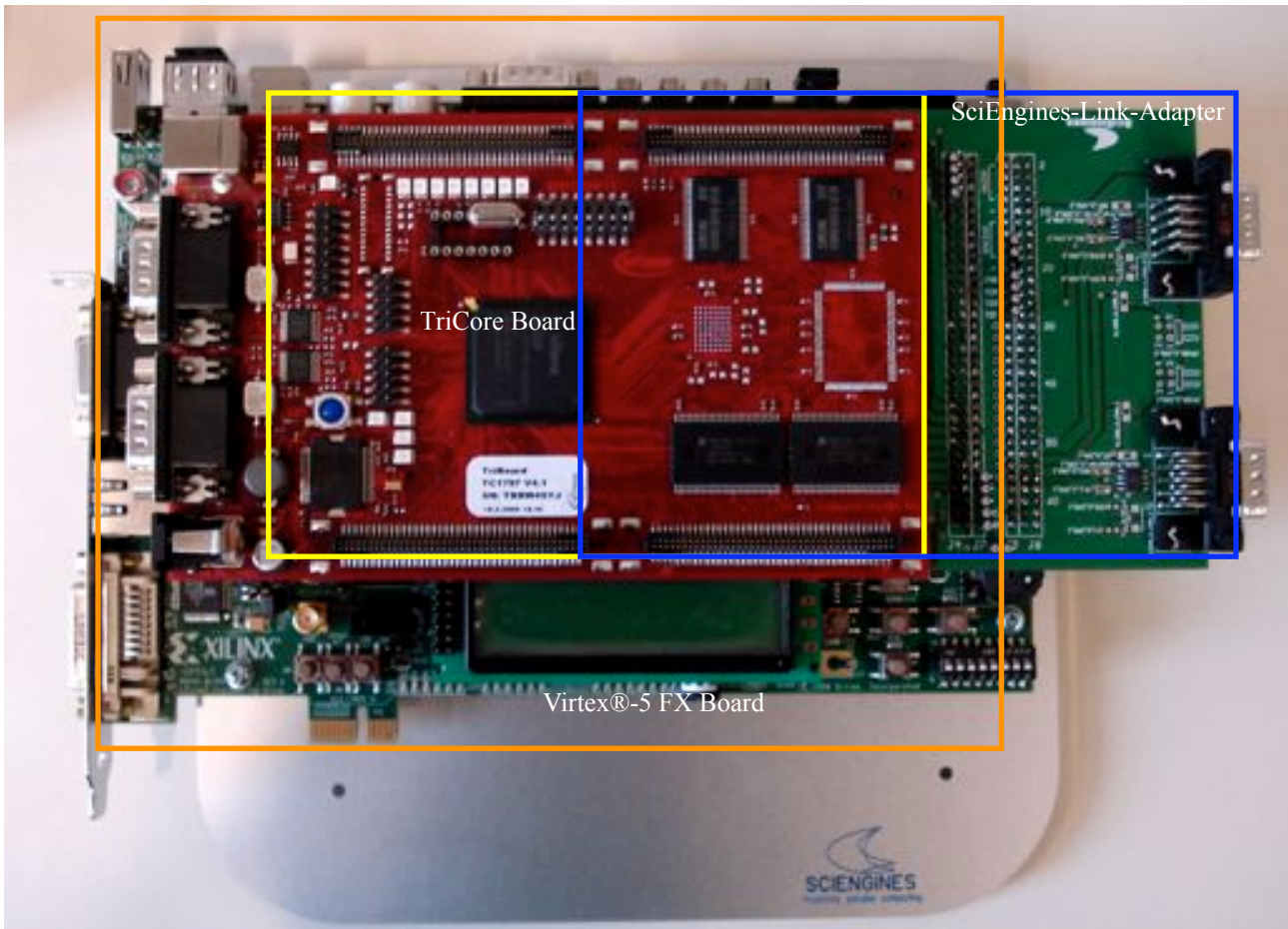


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Overview

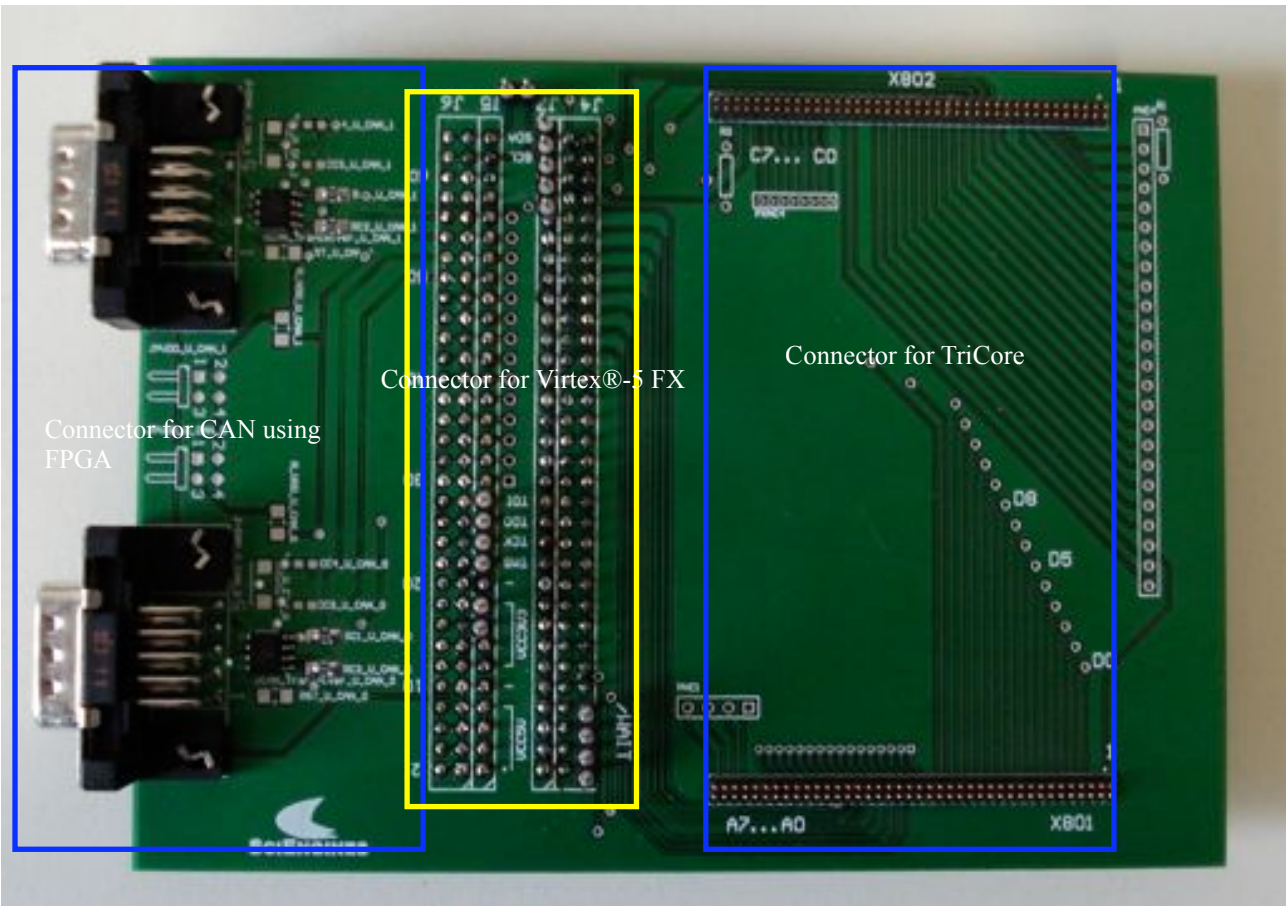


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SciEngines Adapter Overview



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Getting Started

Thank you for purchasing our product.

Step 1 Please unpack all parts



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Step 2 Follow the installation manuals of Xilinx® and Infineon®.

In case of questions contact info@sciengines.com, This document may be updated you will find additional information on our website as soon as it becomes available:

<http://www.sciengines.com>